REMARKS

I. Claim Objections

Claim 8 was objected to as being dependent from cancelled claim 6; hence, claim 8 has been amended to be dependent from claim 4.

II. Claim Rejection – 35 USC § 103

In a Final Office Action, claims 1-4, 7-11, 14-18, 21, 22, 28 and 30-32 were rejected under 35 USC § 103(a) as being unpatentable over Barkatullah in view of Neal. Applicants present the following arguments with respect to this rejection. In filing a Request for Continued Examination (RCE), Applicants' respectfully request that the Examiner amend claim 8 and consider the following arguments.

A. No delay to avoid a period of data signal mismatch caused by a level shifter is disclosed or suggested in Barkatullah or Neal. Applicants' invention as claimed in the independent claims does not involve clock synchronization as undertaken in Barkatullah and Neal.

With respect to Barkatullah, the Examiner states that:

> "....a clock production circuit (Fig. 7) coupled to the clock source (102) and responsive to the clock signal (core clock) to generate a synchronized clock signal (bus clock) having a triggering edge....the clock production circuit (Fig. 7) is operable to synchronize an arrival of the triggering clock edge at the downstream latch until after an arrival of the rising and falling data edges at the downstream latch..."

With respect to Neal, the Examiner states that:

> "....a clock delaying mechanism (150) to synchronize clock triggering.... a clock source (160) that is used by first domain (400) to synchronize data signals (401a-403a) wherein the clock signal is further delayed via delay element (150) ... level shift both data and clock signal as well as delay the clock signal between domains for synchronization...."

Clock syncrhonization is commonly used in integrated circuits, but is not relevant to Applicants' invention as claimed in the independent claims 1, 10, 16, and 28. More specifically, the claimed "delayed clock signal" is not synchronized with the claimed "clock signal". To the contrary, Applicants' invention, as claimed in the independent claims, includes a delay sufficient to avoid the period of mismatch in the level shifted data signal, with that period of mismatch in the level shifted data signal being caused by the first level shifter. The period of mismatch is described in the independent claims by the claim language of "level shifted data signal has a plurality of rising and falling data edges".

Clock syncrhonization involves syncrhronization of a given clock signal with a reference clock signal. A simple example of this is illustrated in FIG. 4 of Neal and discussed in column 5, lines 16-39. There is shown a reference clock signal 300 (original clock that is an input to the voltage level shifter) and the delayed clock signal 302 (delay introduce by the voltage level shifter). By using a "signal deskewer", such as the signal deskewer 150 of FIG. 5, the delayed clock signal 302 is moved forward or backward to be concident with the original signal 300. This moved and synchronized clock signal is shown as signal 304 in FIG. 4.

In independent claims 10 and 16 and dependent claims 2 and 30, Applicants' recite the use of a second level shifter to generate a level shifted clock signal. Neal does teach using a level shifter for the clock signal, as well as using a level shifter for the data signal. In the synchronization with the original clock signal 300, Neal teaches that the clock delay introduced by the voltage lever shifter for the clock signal is to be eliminated through clock synchronization. This leads to two distinctions:

(1) With respect to independent claims 1, 10, 16 and 28, in Neal the delay introduced by the clock level shifter at most would compensate for the delay introduced by the level shifter for the data signal (if the delay was not eliminated in Neal); however, that delay is insufficient by itself to block the period of signal

mismatch caused by the level shifter for the data signal. Applicant's invention, as claimed in the independent claims, recites the delay element which adds sufficient delay to allow the downstream latch to block a period of mismatch in the data signal.

(2) With respect to independent claims 10 and 16 and dependent claims 2 and 30 reciting the second level shifter, the introduced clock delay of Applicants' invention not only includes the clock delay of the delay element, but also includes the clock delay of the second level shifter. Hence, the clock delay of the second level shifter is kept and used in Applicants's claimed invention, not eliminated by clock synchronization as taught by Neal.

In summary, the delay element of Applicants' invention introduces intended delay which is sufficient to eliminate the period of data signal mismatch. No such teaching is found in Neal.

In Barkatullah, clock synchronization becomes more involved, because of frequency translation in which there is a 2/N ratio of the bus clock signal to the core clock signal created by selecting every N/2 cycles of the core clock signal - there is some unrelated discussion as to which phase of the clock signals to use (e.g., see clock waverforms 201 and 202 in FIG. 6A). The Examiner recognizes that there is no delay element in Barkatullah. Since there is no mismatch in a data signal from a level shifter in Barkatullah, then there is no need for the delay element to generate the delayed clock signal. Instead, the Examiner cites Neal for the delay element, which is not related to Applicants' delay element as described above.

In summary, neither Barkatullah and Neal, singly or in combination, disclose a delay element that delays a clock signal, which is used by a flip-flop at the input of a level shifter, to create a delayed clock signal, so as to block a period of signal mismatch caused by the level shifter by having a downsteam latch in a close state when receiving

the period of signal mismatch and then triggering an open (transparent) state of the downstream latch with a triggering clock edge of the delayed clock signal after the arrival of signal mismatch. Neither Barkatullah and Neal, singly or in combination, disclose a delay element to delay a clock signal, with or without the delay of the second level shifter, to a sufficient degree to avoid the period of signal mismatch caused by a level shifter.

B. No downstream latch with open and close state in Barkatullah or Neal.

With respect to FIG. 8C of Barkatullah, the Examiner refers to the three series D flip-flops as DFF1, DFF2, and DFF3. Applicants will adopt the Examiner's characterization of these components in the discussion below. First, the Examiner takes two D flip-flops (DFF1 and DFF2) and states that this is Applicants' single claimed flip-flop. Second, the Examiner equates a third D Flip-flop (DFF3) to Applicants' "downstream latch having an open state and a close state". In doing so, the Examiner claims that the D flip-flop (DFF3), like Applicants' downstream latch, has an open state and a close state. This is a technically incorrect characterization of a flip-flop, with the proper description of a flip-flop being provided in paragraph 0016 of Applicants' specification, which will be repeated here:

> "With respect to the master-slave flip-flop 42, the master and slave latches 44 and 46 each have an open and a close state. The latches 44 and 46 pass through the data when in the open (transparent) state and hold (latch) the data when in the close state. When the master latch 42 is in its close state, it is holding the Data1 signal acquired from the previous clock phase. At the same time, the slave latch 46 is in the open state and is passing the Data1 signal held by the master latch 42 through to the flip-flop's output as the Data2 signal. When the clock phase is reversed, the master latch 44 switches to its open state to acquire new Data1 signal and at the same time the slave latch 46 switches to its close state of holding the previous-provided Data1 signal and continuing to provide it at the output of the flip-flop 42 as the Data2 signal. Hence, the master

and slave latches operate "out-of-phase". The rising clock edge of the clock signal shown in FIG. 4 may be used to reset the master latch 44 to its open state and the falling clock edge of the clock signal may be used to reset the slave latch 46 to its open state. Generally, the flip-flop 42 may introduce a one clock cycle delay in the Data1 signal to generate the Data2 signal."

Although each latch (master or slave) of the flip-flop (including a D flip-flop), has an open state, when the operation of the flip-flop is taken as a whole, a flip-flop does not have an open state, as made clear by the above-described "one clock cycle delay" of the flip-flop. This one clock cycle delay does not occur with the downstream latch, because during an open state of the dowstream latch the signal passes without delay and during the close state, the signal (including the period of signal mismatch) does not pass.

In summary, a flip-flop, including a D flip-flop, is not a simple, single latch having an open (transparent) state and close (hold or latch) state, but is a component that functions in a much different way, as described above. The downstream latch of Applicants' invention at the output of the level shifter operates with a clocking delay relative to the flip-flop at the input of the level shifter to block a period of mismatch in the level shifted data signal.

No downstream latch is disclosed in Neal; hence, neither Barkatullah or Neal, singly or in combination discloses a downstream latch at the output of a level shifter.

C. Domains with different clock frequencies in Barkatullah.versus domains with different voltage levels and voltage level shifters in Applicants' invention

FIG. 7 of Barkatullah shows a circuit for generating a bus clock signal, with one of the inputs being a core clock signal with a 2/N ratio between the bus clock signal to the core clock signal (column 2, lines 65-67, also FIG. 6A). DFF1 and DFF2 are provided

a clock signal with one frequency (core clock) and DFF3 with another frequency (bus clock). Hence, Barkatullah is concerned with providing two clock signals of different frequencies to different domains, the bus clock domain and the core clock domain, as shown in FIG. 1. There are not two domains supplied with different supply voltages in Barkatullah; hence, there are no voltage level shifters, as the Examiner noted. To the contrary, Applicants' independent claims 1, 10, 16, 28 a "first supply voltage source" and a "second supply voltage source" and "a first level shifter".

Moreover, Applicants "clock signal" provided to the flip-flop has the same frequency as the "delayed clock signal" provided to the downstream latch, because they are the same signal but the delay introduced by the "delay element". In other words, the delay element does not change frequency, nor would Applicants' conveter circuit work if the frequency was changed. Hence, Barkatullah, with the exception of the clock source, does not teach any of the recited elements of Applicants' independent claims 1, 10, 16, 28.

D. Summary

Neither Barkatullah and Neal, singly or in combination, dislcose:

(1) a downstream latch at an output of a level shifter, with the level shifter being interposed between a flip-flop and the downstream latch; or

(2) a delay element to delay a clock signal used by the flip-flop, with the downstream latch using a triggering clock edge of the delayed clock signal to switch the downstream latch from a close state to an open state after an arrival of the rising and falling data edges at the downstream latch.

In independent claim 28 the term "downstream slave latch" is used instead of "downstream latch".

III. Conclusion

Claims 1-4, 7-11, 14-18, 21, 22, 28 and 30-32 are pending. In view of the foregoing amendments and arguments, Applicant submits that the pending claims are in condition of allowance. Early issuance of Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

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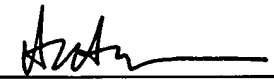

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